Fiber-Interconnect Silicon Chiplet Technology for Self-Aligned Fiber-to-Chip Assembly

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***Abstract*—A passive self-alignment and assembly approach for optical fibers is proposed and demonstrated using a combination of silicon micromachining and 3D printing to achieve efficient and accurate near-vertical coupling to an SOI substrate with monolithic ridge waveguides and grating couplers. The alignment process is repeatable and the peak efficiency is comparable to the active fiber alignment efficiency (86% or -0.67 dB of that obtained from active alignment). The overall alignment accuracy is in the submicron range due to the formation of mechanical self-aligning structures. The overall approach is compatible with numerous applications, including fiber-to-chip and fiber-to-package assemblies as well as in the testing of photonic devices.**

***Index Terms*—optical fiber, optical alignment, passive alignment, fiber array, fiber coupling**

I. Introduction

HETEROGENEOUS integration of electronics with photonics is a promising solution to meet the high-bandwidth, low-latency, and low-energy consumption needs of modern computing systems. Optical fibers, which offer extremely low loss, are especially critical in long-haul applications as well as in the shorter distances found in data-centers and in high-performance computing (HPC). In the latter applications, photonic packaging, assembly, and interfacing to silicon electronics play a critical role in determining overall module performance, energy consumption, and cost. In order to create seamless polylithic integration of photonics and electronics, advances in packaging and assembly are critical. In particular, the accurate alignment and assembly of fibers or fiber arrays to a photonic integrated circuit (PIC) are crucial steps to realize high-efficiency optical packaging and integration [1]. Common fiber alignment techniques include active alignments and passive alignments. With typical alignment accuracy of approximately 100 nm, active alignment schemes require a complex setup consisting of a laser light source and a photodetector, with alignment adjustments realized through the use of a microscope and a rotational stage [2]. The fiber/fiber-array is aligned and assembled serially, which is not time efficient. On the other hand, passive alignment relies on the placement of fibers onto properly designed mechanical structures with a typical alignment accuracy of approximately 1 μm. While this is a lower alignment accuracy than active alignment, it is more time efficient and amenable to scaling. Some passive alignment techniques include V-grooves [3], [4], plugs [5], ferrules [3], and light-splitting techniques [6] that only work for lateral coupling, e.g. edge coupling of fibers to waveguides, evanescent coupling of stripped fibers to waveguides, or coupling fibers mounted parallel to grating surfaces with the assistance of mirrors [6], [7], and thus they do not accommodate all fiber integration schemes. Passive alignment structures for vertical coupling have also been proposed [8], but they typically only work for coupling at a single location and thus they are not scalable. In this letter, a passive fiber-array alignment and assembly approach using Fiber-Interconnect Silicon Chiplet Technology (FISCT) is proposed. FISCT consists of two key elements: 1) a silicon carrier with integrated lithographically defined mechanical self-aligning features and through-vias, and 2) 3D printed fiber ferrules that reside within the vias of the silicon carrier. FISCT enables massive precision self-alignment and assembly of optical fibers onto a package-substrate or a photonic chip, and it is compatible with flip-chip bonding technology. The design and fabrication of the FISCTs are versatile and scalable to accommodate various topologies and packages. The proposed FISCT has the potential in applications that include permanent or temporary fiber attachment. Note that the fiber chiplet concept aims to co-exist with the recent trends in digital electronics in which dice of heterogeneous functionality and materials (i.e., chiplets) are densely interconnect using 2.5D or 3D heterogeneous integration [9], [10]. The aim is to extend the chiplet concept to photonic devices and interconnections.

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II. Structure

The general concept of FISCT is illustrated in Fig. 1(a). A polylithic integration platform (Heterogeneous Interconnect Stitching Technology (HIST) [9]) is formed using electrical and optical stitch chips. The electrical stitch chips, in the simplest form, provide high-density and low-energy connectivity between neighboring dice, while photonic stitch chips provide near-logic E-O/O-E conversion and interfacing to optical fibers. In this letter, we address the technology challenges in interfacing a massive number of optical fibers to a photonic stitch chip with integrated waveguides and diffractive optical couplers using the FISCT approach [9]. Figures 1(b) and 1(c) illustrate details of the FISCT concept.

The design of FISCT is flexible and can be easily modified based on PIC design. The structure is composed of a Si

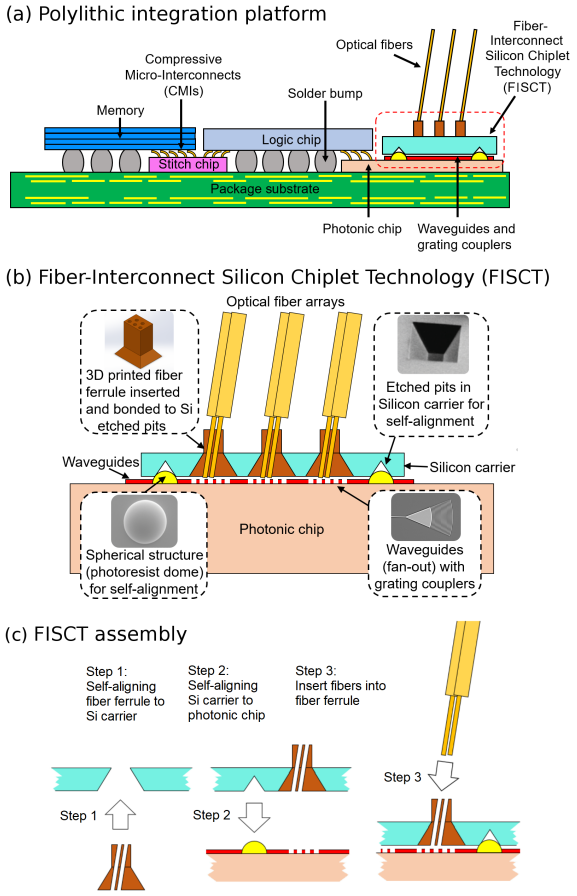

Fig. 1. (a) A conceptual view of the proposed Fiber-Interconnect Silicon Chiplet Technology (FISCT) in the polylithic integration [9], [10]; (b) an enlarged figure shows the details of the FISCT cross-section; and (c) the FISCT assembly process.

carrier substrate, self-alignment structures (etched pits and photoresist domes) [11], [12], and fiber ferrules printed by 3D laser lithography (two-photon polymerization). The Si carrier is lithographically patterned and wet etched resulting in etched pits of two sizes. The small pits are self-aligned to the reflowed photoresist domes deposited on the PIC resulting in positive self-alignment structures (PSAS) [11], [12]. The larger pits are fully etched through the Si substrate, and the laser-printed fiber ferrules are inserted within the through-Si pits and self-align with the pits due to complementary geometries. The fiber ferrules can be secured using epoxy, polymer, or mechanical latches. A fiber placement aid, which is also printed by 3D laser lithography, is placed on top of the fiber ferrules for easier fiber insertion. Segments of the cleaved optical fibers without their coating are inserted into the fiber ferrules, which are fabricated with a pre-defined incline angle with respect to the normal, until they reach the surface of the PIC where they are self-aligned with the grating couplers.

III. Fabrication

The fabrication of the current FISCT approach can be divided into two parts: the chemically etched Si carrier and the 3D printed fiber ferrules (which are then inserted into the silicon carrier). Once formed, FISCT is self-aligned and assembled on a Silicon-On-Insulator (SOI) substrate with integrated ridge waveguides and surface-relief grating couplers. Specifically, the reflowed photoresist domes on the SOI substrate self-align with the smaller pits on the silicon carrier. Since the smaller pits are also lithographically aligned with the pits that hold the fiber ferrules, the fibers become aligned with the grating couplers on the SOI substrate. The details of the fabrication process are described in the following sections.

A. Si Carrier

The process starts with a 300 μm thick, $\langle 100 \rangle$-oriented, and double side polished Si wafer. First, a 200 nm thick Si_3N_4 layer is deposited on both sides of the Si carrier substrate using low-pressure chemical vapor deposition (LPCVD) followed by pit lithographic openings on one side of the wafer. Next, the patterned wafer is placed in a reactive ion etching (RIE) chamber to etch away the exposed Si_3N_4 layer. After photoresist removal, a patterned Si_3N_4 layer is revealed, which serves as the wet etch mask for the exposed Si. The wafer is next immersed in a 45% KOH bath at 90°C for 4 hours resulting in etched pits in the Si substrate. Note that during this process step, two different sizes of pits are formed simultaneously, and thus, all pits are lithographically self-aligned. The resulting pit size simply depends on the size of the windows in the Si_3N_4 hard mask.

B. 3D Printed Fiber Ferrules

The next step is to fabricate the 3D printed fiber ferrules. The ferrule structure is first designed using Solidworks. The bottom portion has a tapering angle of 54.7° corresponding to the angle between $\langle 100 \rangle$ and $\langle 111 \rangle$ crystallographic planes of the Si carrier. A channel through which the fiber is inserted is formed within the fiber ferrule; the channel tilt angle (9°) matches the optimal fiber coupling angle and is pre-determined during the design phase. The fiber locations relative to the grating couplers should be properly designed based on the interlayer gap between the Si carrier and the SOI substrate. The design is then transferred to a Nanoscribe laser lithography system, which is based on two-photon polymerization. The fiber ferrules are printed using in-house IP-S resist on a conductive substrate (indium thin oxide (ITO) or silicon) and the exposed structures are developed in SU8 developer for 20 min. The fiber ferrules can be printed in a 2D array with the same pitch as the through-Si etched pits in the Si carrier substrate, which makes the final assembly relatively simple. The assembled FISCT can be secured using fibers with coatings as latches (for proof of concept) or using photoresist/epoxy as adhesives. The Si carrier has a yellow sheen due to the presence of the thin Si_3N_4 layer.

C. Ridge Waveguide and Grating Formation

The SOI substrate consists of a 2D array of passive photonic circuits. As a test circuit, two focusing grating couplers are connected by a ridge waveguide. The optical signal from the input fiber is coupled into the ridge waveguide via one grating

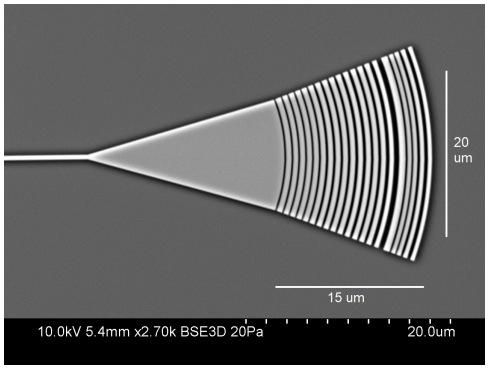

Fig. 2. SEM image of the fabricated focusing grating coupler.

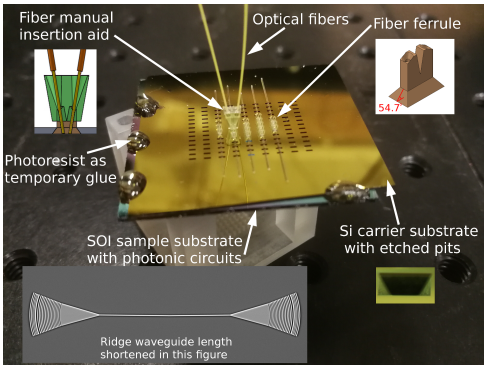

Fig. 3. Optical testing setup after aligning the passive FISCT to the SOI sample substrate.

coupler. The signal would then propagate along the ridge waveguide and diffract out once it reaches the second grating coupler. The out-diffracted signal is then launched into the output fiber. The circuits with alignment marks are fabricated using an SOI wafer with a 250 nm thick device layer and a 3 μm thick buried oxide layer. The gratings, ridge waveguides and alignment marks are patterned in HSQ negative resist using electron-beam lithography (EBL) and fully etched in an inductively coupled plasma (ICP) chamber. A scanning electron microscopy (SEM) image of the fabricated grating is shown in Fig. 2. The resulting grating couplers have a theoretical fiber coupling efficiency of 30% (-5 dB), which can be improved by shallow etching the grating grooves but would require two-step EBL. However, the fabrication of high-efficiency grating couplers is not the focus of this research. Some high-efficiency grating coupler designs can be found in [13].

Once the gratings and waveguides are fabricated, photoresist domes (i.e., PSAS) are formed by first spin-coating a positive photoresist and then patterning photoresist cylinders using photolithography. The photoresist cylinders are reflowed yielding domes with desired height and radius. The size of the photoresist cylinder, e.g. radius and film thickness, should be co-designed with the Si etched pit openings [11]. The current PSAS-pit combination results in an interlayer gap of 20 μm between the Si carrier and the photonic chip. Index-matching gel can be applied to the grating locations prior to FISCT assembly during which a force is applied onto the Si carrier by the flip-chip bonder to deform the gel droplet and fill the gap between the grating and the bottom of the ferrule.

IV. Testing

The gratings are first characterized using the fiber active stage alignment. The light source is swept from 1560 nm to 1630 nm. The fabricated grating couplers were optimized for a wavelength of 1550 nm. The measured diffraction peak occurs at a wavelength of 1610 nm due to fabrication variations.

After obtaining the reference measurements using the active stage alignment, the fabricated FISCT is picked up using a flip-chip bonder and 'dropped' above the SOI substrate. The PSAS-pits combination will ensure that FISCT and the SOI substrate will be precisely aligned and separated by a pre-defined interlayer gap. A small force is applied on top of the fiber ferrules while photoresist is dispensed on the edges of the aligned substrates to temporarily adhere the two parts together. The force is maintained until the photoresist has solidified. During this process, the PSAS also prevents the relative sliding of the substrates. A fiber insertion aid is placed on top of the fiber ferrule to assist fiber insertion by hand with the unaided eye, although, we envision fibers (or fiber ribbons) inserted with a high-speed and coarse fiber placement tool. The input and output fibers are subsequently inserted into the corresponding channels of the fiber ferrule.

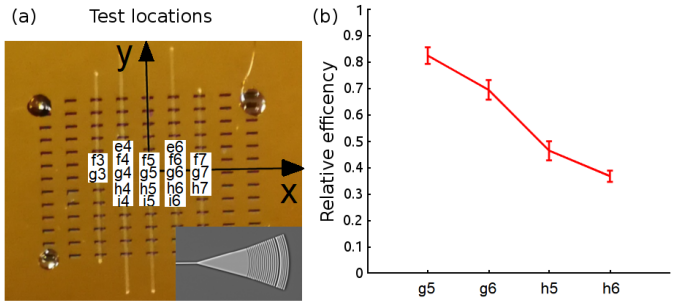

Fig. 4. (a) Test locations of the photonic circuits and (b) measurement data (including 95% confidence interval) at locations g5, g6, h5, and h6 including their symmetric locations.

In order to counterbalance possible fabrication variations and predict misalignment tolerances, the locations of the photonic circuits on the SOI substrate are shifted relative to the pit locations on the Si carrier in 1 μm increments along each of the x and y directions, and the amount of the shift is based on the coordinate of the pit-circuit pair as shown in Fig. 4(a).

Figure 5 shows the measurement results at 3 locations, namely g5 (no shift), g6 (circuit shifted 1 μm in the $+x$ direction), and h5 (circuit shifted 1 μm in the $-y$ directions). The left set of figures show the data measured in volts, which is the output of the photodetector, and the right column shows the relative intensity in dB. The black solid curves correspond to the active stage alignment while the blue dashed curves are obtained using the proposed passive FISCT. At location g5, FISCT and the photonic circuit are designed to be perfectly

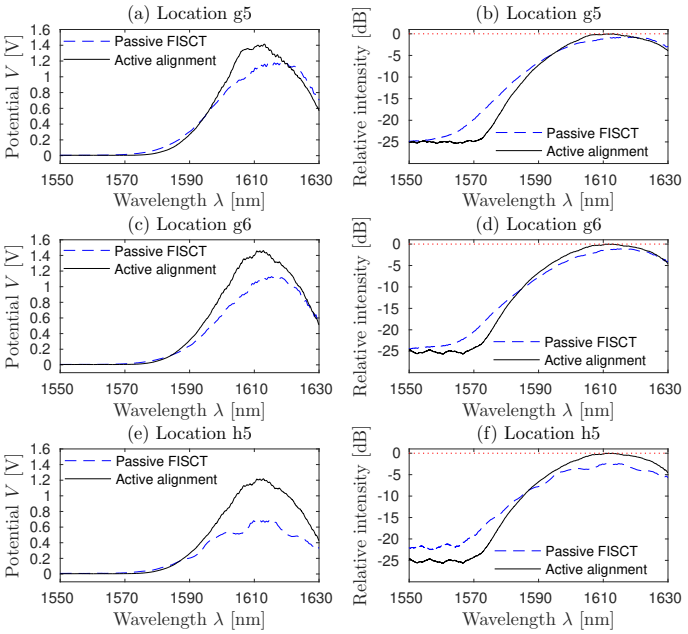

Fig. 5. Comparison of the measurement results obtained from the passive FISCT and the active stage alignment at three testing locations.

aligned, and the peak signal (filtered data) measured by FISCT is approximately 86% (-0.67 dB) of that measured by the active stage alignment. The slightly lower efficiency measured by FISCT is probably due to the uncontrolled z location of the fiber inside of the ferrule in the current demonstration, and thus the x location of the fiber tip may shift from the ideal aligned position due to the 9° tilt angle. Since the fiber is only allowed to move along a line in the fiber ferrule while it can move freely in space under active stage alignment, the extra degree of restriction causes the intensity of the passive method to be smaller. The peak signal at locations g6 and h5 is approximately 75% (-1.2 dB) and 50% (-3 dB) of the reference peak at the corresponding location, respectively. This implies that the misalignment along the x direction has a smaller effect than the misalignment along the y direction. This is because shifting the fiber along the y direction will break the symmetry and affect the coupling mode. Since the fiber mode is approximately 10 μm in diameter, and the focusing grating has a length of roughly 15 μm, shifting along the x direction is tolerable.

The measurement of the passive FISCT is repeatable after retracting and re-inserting the fibers. For example, Fig. 4(b) shows multiple experimental data points at locations g5, g6 (and its symmetric location g4), h5 (and its symmetric location f5), and h6 (and its symmetric locations f4, h4, and f6). The red line traces the mean of the repeated passive measurement data; 95% of the measured data is within the range indicated by the error bars. Furthermore, high intensity can be obtained by simply inserting the fibers into the fiber ferrules and slightly adjusting the fiber polarization, which is more time-efficient compared with the active alignment schemes. The fiber is inserted until it reaches the SOI substrate; the fiber end facet and the gratings were found to be undamaged. By properly designing the fiber ferrules and the Si carrier substrate, fiber arrays can be aligned using the proposed FISCT.

V. Conclusion

A passive Fiber-Interconnect Silicon Chiplet Technology (FISCT) is proposed and demonstrated to achieve accurate and reliable fiber-to-grating alignment, assembly, and packaging. It enables time-efficient alignment, assembly, and packaging of fibers or fiber arrays, and it is suitable for testing, prototyping, and permanent attachment of fibers to chips or packages.

Acknowledgement

This work was performed in part at the Georgia Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (ECCS-1542174). This work was supported in part by NSF Grant ECCS-1810081.

References

[1] A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbelaere, "A grating-coupler-enabled CMOS photonics platform," *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 3, pp. 597–608, May/Jun. 2011.

[2] M. Carminati, S. Grillanda, P. Ciccarella, G. Ferrari, M. J. Strain, M. Sampietro, A. Melloni, and F. Morichetti, "Fiber-to-waveguide alignment assisted by a transparent integrated light monitor," *IEEE Photon. Technol. Lett.*, vol. 27, no. 5, pp. 510–513, Mar. 1, 2015.

[3] T. Barwicz, Y. Taira, T. W. Lichoulas, N. Boyer, Y. Martin, H. Numata, J.-W. Nah, S. Takenobu, A. Janta-Polczynski, E. L. Kimbrell, R. Leidy, M. H. Khater, S. Kamlapurkar, S. Engelmann, Y. A. Vlasov, and P. Fortier, "A novel approach to photonic packaging leveraging existing high-throughput microelectronic facilities," *IEEE J. Sel. Top. Quantum Electron.*, vol. 22, no. 6, pp. 455–466, Nov./Dec. 2016.

[4] R. Hauffe, U. Siebel, K. Petermann, R. Moosburger, J.-R. Kropp, and F. Arndt, "Methods for passive fiber chip coupling of integrated optical devices," *IEEE Trans. Adv. Packag.*, vol. 24, no. 4, pp. 450–455, Nov. 2001.

[5] A. Sasaki, T. Baba, and K. Iga, "Put-in microconnectors for alignment-free coupling of optical fiber arrays," *IEEE Photon. Technol. Lett.*, vol. 4, no. 8, pp. 908–911, Aug. 1992.

[6] N. Pavarelli, J. S. Lee, M. Rensing, C. Scarcella, S. Zhou, P. Ossieur, and P. A. OBrien, "Optical and electronic packaging processes for silicon photonic systems," *J. Light. Technol*, vol. 33, no. 5, pp. 991–997, Mar. 1, 2015.

[7] R. R. Vallance, L. Shuhe, R. D. Dannenberg, and M. K. Barnoski, "Optical connection of optical fibers to grating couplers," Dec. 29, 2016, US Patent App. 14/714,247.

[8] S. P. Anderson, V. Patel, and D. Piede, "Passively placed vertical optical connector," May 7, 2015, US Patent App. 14/070,962.

[9] X. Zhang, P. K. Jo, M. Zia, G. S. May, and M. S. Bakir, "Heterogeneous interconnect stitching technology with compressible microinterconnects for dense multi-die integration," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 255–257, Feb. 2017.

[10] P. K. Jo, X. Zhang, J. L. Gonzalez, G. S. May, and M. S. Bakir, "Heterogeneous multi-die stitching enabled by fine-pitch and multi-height compressible mircointerconnects (CMIs)," *IEEE Trans. Electron Devices*, 2018.

[11] H. S. Yang, C. Zhang, and M. S. Bakir, "Self-aligned silicon interposer tiles and silicon bridges using positive self-alignment structures and rematable mechanically flexible interconnects," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 11, pp. 1760–1768, Nov. 2014.

[12] ——, "A self-aligning flip-chip assembly method using sacrificial positive self-alignment structures," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 3, pp. 471–477, Mar. 2016.

[13] C. Wan, T. K. Gaylord, and M. S. Bakir, "Grating-assisted-cylindrical-resonant-cavities interlayer coupler," *Appl. Opt.*, vol. 57, no. 18, pp. 5079–5089, Jun. 20, 2018.